UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,759	10/29/2003	Fang-Zhong Chen	15436.247.5.1	7926

22913 7590 08/24/2004

WORKMAN NYDEGGER (F/K/A WORKMAN NYDEGGER & SEELEY)
60 EAST SOUTH TEMPLE
1000 EAGLE GATE TOWER
SALT LAKE CITY, UT 84111

EXAMINER	
NGUYEN, JIMMY	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,759	CHEN ET AL.	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/29/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification of the disclosure is objected to because

Page 7 line 19 base "18" instead of "16".

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashinaga et al (US 5414370).

As to claim 1, Hashinaga et al disclose (figs 1- 3) a system for testing optoelectronic devices, the system comprising:

a burn-in rack (10, fig 1) mountable within a support structure (30, fig 2), said burn-in rack (10) supports a plurality of optoelectronic devices (33, fig 3) during burn-in testing and life testing, said burn in rack (10) with said plurality of optoelectronic devices (33) being disposable in either a burn-in oven (12) or within said support structure (30, fig 2) for life testing, and

a detector assembly (38) mounted to said support structure, said detector assembly comprising a plurality of detectors (38), each of said plurality of detectors (38)

aligning with one of said plurality of optoelectronic devices (33) to detect an output of each of said plurality of optoelectronic devices (33) during the testing.

As to claim 2, Hashinaga et al disclose (figs 1- 3) a system as recited in claim 1, wherein system further comprising a computer in electrical communication with at least one of burn in rack (10) and detector assembly (38).

As to claim 3, Hashinaga et al disclose (figs 1- 3) a system as recited in claim 2, wherein computer (46) controls life testing and burn in testing.

As to claims 4, 7, 14, Hashinaga et al disclose (figs 1- 3) a system as recited in claim 1, wherein burn in rack comprises:

A rack base (10) that supports a circuit board (14); and

At least one diode support (16) disposed form and supported by rack base, at least one diode support supporting plurality of optoelectronic devices (33).

As to claims 5, 8, Hashinaga et al disclose (figs 1- 3) a system as recited in claim 1, wherein plurality of detectors (38) are organized in an array.

As to claims 6, 12, 13, 20, Hashinaga et al disclose (figs 1- 3) a system and a method for testing optoelectronic devices, the system and method comprising:

a burn-in rack (10) having a plurality of laser diode holders (16) and electrical signal connectors (18) for electrically coupling laser diodes mounted in said holders (16) to a first electrical connector (30),

a test apparatus (12) configured to hold said burn-in rack (10) and having optical detectors (38) arranged to receive light from said laser diodes (33) mounted to said burn in rack (10) and couple output signals from said optical detectors (38) to a second electrical connector (the terminal connect to detecting unit 44),

a computer (46) coupled to said first and second electrical connectors, said computer 946) creating a drive current supplied to each laser diode and measuring the light output from said optical detectors (38).

As to claim 9, Hashinaga et al disclose (figs 1- 3) a system of claim 6, wherein electrical connectors (30) are edge connectors.

As to claim 10, Hashinaga et al disclose (figs 1- 3) a system of claim 6, wherein burn in rack (10) slidably cooperates with test apparatus.

As to claim 11, Hashinaga et al disclose (figs 1- 3) a system of claim 6, wherein burn in rack (10) is capable of being disposed within a burn in oven (12).

As to claim 15, Hashinaga et al disclose (figs 1- 3) a system of claim 6, wherein burn in rack (10) further comprises at least circuit board (14) electrically connected to a plurality of optoelectronic device holders (16) and plurality of optoelectronic devices (33) disposed within plurality of optoelectronic device holders (16).

As to claim 16, Hashinaga et al disclose (figs 1- 3) a system of claim 12, wherein means for detecting comprises a detector assembly having a plurality of detectors (38).

As to claim 17, Hashinaga et al disclose (figs 1- 3) a system of claim 16, wherein plurality of detectors (38) detect electromagnetic waves propagated from plurality of optoelectronic devices (33).

As to claims 18, 21, Hashinaga et al disclose (figs 1- 3) a system of claim 12 and method of claim 20, wherein means for detecting comprises a monitor detector (38) integrated within each of plurality of optoelectronic devices (33).

As to claim 19, Hashinaga et al disclose (figs 1- 3) a system of claim 12. wherein means for delivering comprising a computer (46) electrically connected to plurality of optoelectronic devices (33) and means for detecting.

As to claims 22 - 24, Hashinaga et al disclose (figs 1- 3) the method further comprising step of calibrating integrated detector and optical detectors (by the computer 46) and removing burn in rack (10) and performing a burin process

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen at (571) 272-1965. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.

JN.
August 19, 2004

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800